Electronic Version
Stylesheet Version v1.1.1

DRAM Circuit and its Operation Method

Abstract

A high-density DRAM in a MTBL method which reduces interference noise between bit lines is provided. Duplication of sense amplifiers (SA) and bit switches (BSW) in a conventional MTBL method is eliminated, and one line of sense amplifiers and bit switches (BSW/SA) is arranged between cell areas. Specifically, arrays are horizontally moved and vertically cumulated so as to reduce the areas. Bit line pairs to be connected are alternately interchanged above and below, every one horizontally aligned sense amplifier (SA). Bit lines of a bit line pair 11 cross at one place on the way, and from the cross, a space between the bit lines is wider. Further, bit lines of a bit line pair 16 do not cross each other, and a space between the bit lines is wider on the way. In a new MTBL method, both in the bit lines connected to the same sense amplifier and in the bit lines among adjacent bit lines connected to the different sense amplifiers, a space between the bit lines changes (widens or narrows) before and after the cross. Thus, the interference noise between any adjacent bit lines is decreased.